REMARKS

Claims 1-4, 6-19, and 21-32 remain pending and at issue in the above identified patent application. Of the claims at issue, claims 1, 16, and 32 are independent. Claims 1, 16, and 32 have been amended to clarify the scope of protection sought. In view of the foregoing amendments and the following remarks, reconsideration of the application is respectfully requested.

Claim Objections

Claim 23 was objected to for minor informalities. Claim 23 has been amended to remove the limitations now present in claim 16. The foregoing should eliminate any objection to the claim.

The Rejections under 35 U.S.C. § 103

Independent claims 1, 16, and 32 have been amended to clarify that the processor detects a user event likely to result in a cache miss or when cache miss is not predicted. Claims 1, 16, and 32 were rejected as being unpatentable over Bhatt (US 2002/0073426) in view of Trovato (US 6,445,306), and in further view of Millillo (US 6,834,325). It is respectfully submitted that all claims are allowable over these patents for at least the reasons set forth below.

As amended, independent claims 1, 16, and 32 are directed to a system for efficient storage of data including a processor that directs that data be temporally sorted and stored by comparison of a current time to a time associated with the data, into data that is most likely to be immediately accessed for an application, and data that is most likely to be accessed in the more distant future, wherein the data that is most likely to be immediately accessed is stored in a physical memory, and the data that is most likely to be accessed in the more distant future is stored in a mass storage device. The processor further detects a user event likely to result in a cache miss or when a cache miss is not predicted.

Neither Bhatt, Trovato, nor Milillo, either alone or in combination, teaches or suggests the predictive detection of a user event, such as, for example, an electronic program guide scroll, that may result in a cache miss. In particular, in rejecting the claims, the examiner acknowledges the deficiencies of Bhatt and Trovato and relies upon Milillo stating that Milillo discloses a processor that "detects usage scenarios likely result in a cache miss." (See Office action, page 5). In contrast, however, while Milillo describes a system that identifies a machine dependent sequential and/or non-sequential memory access and pre-stages records into high speed memory in advance of that memory access. (Milillo, 3:11-16). Milillo fails to teach or suggest the detection of a user event that is likely to result in a cache miss.

Specifically, Milillo is directed to a disk channel cache memory that relies upon a pre-stage bitmap to identify blocks of data from mass storage disks. (Milillo, 6:13-19). The identified blocks are preloaded into the disk channel cache memory where they are available to satisfy a read request from a host computer. (Id.). The pre-stage bitmap "is a set of data transmitted from the host computer to the disk channel processor 111 to identify which blocks of data from the mass storage disks 102 are most likely to be requested by the host processor 101 in

upcoming processing." (Milillo, 6:19-23; emphasis added). In other words, Milillo is predicated on the establishment of a computer generated pre-stage bitmap, and the loading of cache data (e.g., 12 tracks) based solely upon the received bitmap.

Furthermore, as described in Milillo, the channel processor is not required to store the data blocks within cache memory, and any detection of a cache miss is reactive, rather than predictive as claimed. For example, Milillo describes that "if the host computer 101 generates a read request immediately following a bitmap 414 write operation, the disk channel processor 111 may not have had sufficient time to have prestaged the data blocks being requested. In such a situation, the disk channel processor 111 detects the cache 'miss' and retrieves the data block directly from the mass storage device." (Milillo, 7:1-6; emphasis added). Thus, Milillo describes a reactive response to a cache miss, namely the loading of data directly from storage, and fails to teach or suggest a predictive response based upon a user event.

Accordingly, for at least the foregoing reasons, Milillo fails to teach or suggest any user event initiated predictive caching as recited in the present claims.

Therefore, due to the deficiencies in Milillo, it follows that no combination of Bhatt, Trovato or Milillo can render obvious claims 1, 16, 32, or any claims dependent thereon. In particular, because neither Bhatt, Trovato, nor Milillo describes any detection of a user event that may result in a cache miss, no combination of Bhatt, Trovato, and Milillo can obviate the claims.

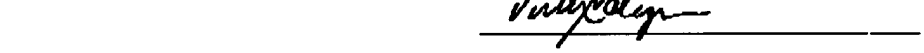
Thus, for at least the foregoing reasons, it is respectfully submitted that claims 1, 16, 32, and all claims dependent thereon are in condition for allowance.

Conclusion

Reconsideration of the application and allowance thereof are respectfully requested. If there is any matter that the examiner would like to discuss, the examiner is invited to contact the undersigned representative at the telephone number set forth below.

Should any fees be associated with this submission, please charge Deposit Account 50-0383.

Respectfully submitted,



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